WHAT IS CLAIMED IS:

1. A memory controller emulator for controlling memory devices in a memory system comprising:

a counter for generating a plurality of address values; and

a plurality of storage devices coupled to the counter for storing memory address information, memory data to be stored in the memory devices, and memory commands for controlling operation of the memory devices, each of the plurality of storage devices configured to output data stored therein based upon address values received from the counter.

2. The memory controller emulator of claim 1, wherein the memory controller emulator is a programmable logic device.

3. The memory controller emulator of claim 2, wherein the storage devices are ROMs.

4. The memory controller emulator of claim 3, wherein the memory commands, memory address information, and memory data stored in the ROMs are programmable by a computer.

5. The memory controller emulator of claim 1, wherein the memory data includes error correction code information.

6. The memory controller emulator of claim 1, wherein the memory address information includes row address information, column address information, and bank address information.

7. The memory controller emulator of claim 6, wherein the memory address information includes chip select information.

8. The memory controller emulator of claim 1, wherein one of the storage devices stores scope synchronization information to be output to an oscilloscope.

9. The memory controller emulator of claim 1, and further comprising:

a clock input for receiving a clock signal; and

a plurality of phase-locked loops coupled to the clock input for generating a plurality of clocks signals at different frequencies and different phase shifts.

10. The memory controller emulator of claim 9, wherein the frequencies and phase shifts of the clock signals generated by the plurality of phase-locked loops are programmable.

11. The memory controller emulator of claim 9, wherein the counter is coupled to a first one of the phase-locked loops, and wherein the counter is configured to output address values at transitions of the clock signal generated by the first phase-locked loop.

12. The memory controller emulator of claim 9, and further comprising:

a plurality of output registers, each output register coupled to one of the storage devices and to one of the phase-locked loops, each output register configured to latch the output of the storage device at a clock transition of the clock signal generated by the phase-locked loop coupled to the output register.

13. The memory controller emulator of claim 1, wherein the plurality of address values include a start address and an end address, and wherein the start address and the end address are programmable.

14. The memory controller emulator of claim 1, wherein the memory data is stored in a first and a second storage device that each output memory data at a first output rate, the memory controller emulator further comprising:

a multiplexer for selectively outputting data from the first and the second storage devices;

a register for receiving memory data output by the multiplexer, the register outputting the received memory data at a second output rate that is about double the output rate of the first output rate.

15. The memory controller emulator of claim 1, wherein a first and a second storage device each output strobe signals at a first output rate, the memory controller emulator further comprising:

a multiplexer for selectively outputting strobe signals from the first and the second storage devices;

a register for receiving strobe signals output by the multiplexer, the register outputting the received strobe signals at a second output rate that is about double the output rate of the first output rate.

16. A method of emulating a memory controller for controlling memory devices in a memory system comprising:

storing memory address information, memory data to be stored in the memory devices, and memory commands for controlling operation of the memory devices;

automatically generating a plurality of sequential values; and

outputting stored memory address information, memory data, and memory commands, based upon the generated sequential values.

17. The method of claim 16, wherein the method is implemented with a programmable logic device.

18. The method of claim 17, wherein the memory address information, memory data, and memory commands are stored in at least one ROM of the programmable logic device.

19. The method of claim 16, and further comprising:

inputting memory address information, memory data, and memory commands, into a computer; and

downloading the memory address information, memory data, and memory commands to a programmable logic device.

20. The method of claim 16, wherein the memory data includes error correction code information.

21. The method of claim 16, wherein the memory address information includes row address information, column address information, and bank address information.

22. The method of claim 21, wherein the memory address information includes chip select information.

23. The method of claim 16, and further comprising:

storing scope synchronization information; and

outputting stored scope synchronization information to an oscilloscope based upon the generated sequential values.

24. The method of claim 16, and further comprising:

receiving a clock signal; and

generating a plurality of clocks signals at different frequencies and different phase shifts with a plurality of phase-locked loops.

25. The method of claim 24, wherein the frequencies and phase shifts of the clock signals generated by the plurality of phase-locked loops are programmable.

26. The method of claim 24, and further comprising:

outputting the sequential values at transitions of the clock signal generated by a first one of the phase-locked loops.

27. The method of claim 16, wherein the plurality of sequential values include a start value and an end value, and wherein the start value and the end value are programmable.

28. The method of claim 16, and further comprising:

storing the memory data in odd and even banks, the odd and even banks each configured to output memory data at a first output rate; and

providing a register for receiving memory data output by the odd and even banks, the register configured to output the received memory data at a second output rate that is about double the output rate of the first output rate.

29. The method of claim 16, and further comprising:

storing strobe signals in odd and even banks, the odd and even banks each configured to output strobe signals at a first output rate; and

providing a register for receiving strobe signals output by the odd and even banks, the register configured to output the received strobe signals at a second output rate that is about double the output rate of the first output rate.

30. A memory controller emulator comprising:

at least one storage device for storing signal information representing signals transmitted from a memory controller to a memory module; and

an address generator coupled to the at least one storage device, the address generator configured to output address information, the at least one storage device configured to output signal information based upon address information received from the address generator.